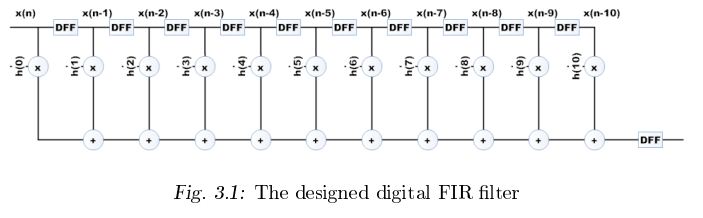
**3. MODELING AND SIMULATION:**

As shown in the section 2 digital filters consist of a lot of constant multipliers. Multiplying two numbers uses a lot of hardware resources. The central problem then becomes substituting the full multipliers by an optimized sequence of shift, additions and subtractions. The whole filter is shown in figure 3.1 .The frequency response of the filter is shown in figure 3.2 and the filters coefficients and their 2’s complement representation and CSD representation are shown in table 3.1 and table 3.2 respectively.

DFF: Delay Flip Flop

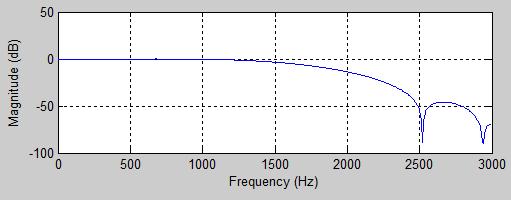


Fig. 3.2: Frequency response of designed filter.



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**Canonical Signed Digit (CSD) Based Low Power FIR Filter Design**

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